This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Original) A hierarchical test control network for an integrated circuit, comprising:

a top-level test control circuit block, said top-level test control circuit block comprising a chip access port (CAP) controller; and

a plurality of lower-level test control circuit blocks connected to said top-level test control circuit block in a hierarchical structure, each of said lower-level test control circuit blocks comprising a socket access port (SAP) controller;

wherein test operation is transferred downward and upwards within said hierarchical structure.

2-14. (canceled).